IN THE SPECIFICATION:

Please replace paragraph number **[0001]** with the following rewritten paragraph:

[0001] This application is a continuation of application Serial No. 10/218,335, filed August 13, 2002, ~~pending~~ now U.S. Patent 6,630,733, issued October 7, 2003, which is a continuation of application Serial No. 09/943,845, filed August 30, 2001, now U.S. Patent 6,445,067, issued September 3, 2002, which is a continuation of application Serial No. 09/539,092, filed March 30, 2000, now U.S. Patent 6,329,710 B1, issued December 11, 2001, which is a continuation of Serial No. 09/294,185, filed April 19, 1999, now U.S. Patent 6,087,720, issued July 11, 2000, which is a continuation of application Serial No. 09/047,726, filed March 25, 1998, now U.S. Patent 5,907,184, issued May 25, 1999, which is a continuation of application Serial No. 08/713,798, filed September 13, 1996, now U.S. Patent 5,763,945, issued June 9, 1998.

Please replace paragraph number **[0005]** with the following rewritten paragraph:

[0005] In a conventional lead frame configuration, some of the lead fingers carry a signal to the semiconductor device while others provide a power source or a ground. ~~In an~~In a LOC frame configuration, the lead fingers likewise provide a signal to the semiconductor device but the power source and ground are typically provided by bus bars. The bus bars typically form elongated contact portions in close proximity to the one or more lines of bond pads on the active surface of the semiconductor device, each bus bar having the contact portion thereof extending perpendicular to the other lead fingers and over the active surface of the semiconductor device.

Please replace paragraph number **[0020]** with the following rewritten paragraph:

[0020] Referring to drawing Fig. 2, the V_{cc} lead 34 has been extended and routed around a portion of the periphery of semiconductor device 14. Similarly, the V_{ss} lead 36 has also been extended and routed around an opposite portion of the periphery of semiconductor device 14. The V_{cc} and V_{ss} leads 34, 36, respectively, extend substantially parallel to the sides of

the semiconductor device 14 and substantially perpendicular to a portion of the lead fingers 18 of the lead frame 12. Each of the V_{cc} and V_{ss} leads 34, 36, respectively, has a single lead end 20 at a proximal end that terminates near or adjacent the semiconductor device 14 and a single lead connection 21 at a distal end. In this manner, the position and number of bond pads 38 are not limited to a single location on the periphery of semiconductor device 14 nearest the lead end of the V_{cc} lead 34 or V_{ss} lead 36. Rather, the bond pads 38 requiring a ground or power source may be located anywhere along either the sides of the semiconductor device 14 forming the periphery of the semiconductor device 14 or located anywhere on the active surface 15 of the semiconductor device 14. In this manner, the V_{cc} lead 34 and V_{ss} lead 36 act much like the bus bars ~~in an~~ in a LOC configured lead frame. The wire bonds 22 extend over the V_{cc} lead 34 and V_{ss} lead 36 between the bond pads 38 and the lead ends 20. Providing the extended V_{cc} and V_{ss} leads 34, 36, respectively, around the periphery of the semiconductor device 14 also helps decrease the number of power and ground buses required within the semiconductor device itself, thereby helping to decrease its size and increase the speed and performance of the semiconductor device 14.

Please replace paragraph number **[0022]** with the following rewritten paragraph:

[0022] In the second embodiment of the present invention, the modified lead frame 12 includes a die paddle 40 to support the semiconductor device 14. The semiconductor device 14 may be adhesively attached to the die paddle 40 by means of thermosetting or thermoplastic adhesive or epoxy paste. The V_{cc} lead 42 extends along the length, a side or first side, of the semiconductor device 14, rather than terminating at a proximal end as the other lead fingers 18, and extends substantially perpendicular with respect to a portion of the lead fingers 18 and at an angle with respect to other lead fingers 18. Similarly, the V_{ss} lead 44 also extends along the opposite length, another side or second side, of the semiconductor device 14 in the same manner as V_{cc} lead 42. As shown, the V_{cc} and V_{ss} leads 42, 44, respectively, extend substantially parallel to each other and to two of the sides of the semiconductor device 14. Unlike the first embodiment of the present invention, the V_{cc} and V_{ss} leads 42, 44 in the present embodiment do

not terminate near the semiconductor device but, rather, are connected at each end thereof to the lead frame 12. Also unlike the first embodiment of the present invention, the V_{cc} and V_{ss} leads 42, 44, respectively, in the second embodiment form a continuous lead along the length of the semiconductor device 14 with each end terminating as a lead connection (not shown). In this manner, the position and number of bond pads 38 are not limited to a single location on the periphery or on the active surface 15 of semiconductor device 14 nearest the lead end of the V_{cc} lead 42 or V_{ss} lead 44. Rather, the bond pads 38 requiring a ground or power source may be located anywhere along the periphery or the active surface 15 of the semiconductor device 14. In this manner, the V_{cc} lead 42 and V_{ss} lead 44 of a conventional lead frame 12 act much like the bus bars ~~in an~~ in a LOC configured lead frame. The wire bonds 22 extend over the V_{cc} lead 42 and V_{ss} lead 44 between the bond pads 38 and the lead ends 20. Unlike the bus bars ~~in an~~ in a LOC configured lead frame, however, the V_{cc} lead 42 and V_{ss} lead 44 of the conventional lead frame 12 do not extend over the active surface 15 of semiconductor device 14. Providing the V_{cc} and V_{ss} leads 42, 44, respectively, around the periphery of the semiconductor device also helps decrease the number of power and ground buses within the semiconductor device 14 itself, thereby helping to decrease its size and increase the speed and performance of the semiconductor device 14.

Please replace paragraph number **[0025]** with the following rewritten paragraph:

[0025] Since the lead frame 12 does not include a die paddle for supporting the semiconductor device 14, the V_{cc} lead 42 and V_{ss} lead 44 can be extended to surround a greater portion of the periphery of the semiconductor device 14, i.e., multiple sides of the semiconductor device 14 or portions thereof. The V_{cc} lead 42 is bifurcated to form a first portion extending along the ends 20 of lead fingers 18 and a side or first side of the periphery of the semiconductor device 14 and a second transverse prong portion 46 to provide a power source along another side or second side of the periphery of semiconductor device 14. Similarly, V_{ss} lead 44 is bifurcated to form a first portion extending along lead ends 20 of lead fingers 18 and another or third side of the periphery of the semiconductor device 14 and a second transverse prong portion 48 to

provide a ground along another or fourth side of the periphery of semiconductor device 14. The V_{cc} and V_{ss} leads 42, 44, respectively, and the transverse prong portions 46, 48, respectively, extend substantially parallel to the sides of the semiconductor device 14. Unlike the prior second embodiment of the present invention utilizing a paddle, in the present embodiment the semiconductor device 14 may be substantially surrounded by the V_{cc} and V_{ss} leads 42, 44, respectively. In this manner, the position and number of bond pads 38 are not limited to a location on the periphery of semiconductor device 14 nearest the lead end of the V_{cc} lead or V_{ss} lead 42, 44, respectively. Rather, the bond pads 38 requiring a ground or power source may be located anywhere along the periphery or the active surface 15 of the semiconductor device 14. In this manner, the V_{cc} lead 42 and V_{ss} lead 44 become much like the bus bars ~~in an~~ in a LOC configured lead frame. The wire bonds 22 extend over the V_{cc} lead 42 and V_{ss} lead 44 between the bond pads 38 and the lead ends 20. Providing the extended V_{cc} and V_{ss} leads 42, 44, respectively, around the periphery of the semiconductor device also helps decrease the number of power and ground buses within the semiconductor device itself, and helps to decrease the size of the semiconductor device 14 and increase the speed and performance of the semiconductor device 14. Unlike the bus bars ~~in an~~ in a LOC configured lead frame, however, the V_{cc} lead 42, V_{ss} lead 44, and prongs 46, 48 do not extend over the active surface 15 of the semiconductor device 14.